3.3V, Precision LVPECL and LVDS Programmable Multiple Output Bank Clock Synthesizer and Fanout Buffer

SY89538L Evaluation Board

General Description

The SY89538L integrated, programmable clock synthesizer and fanout buffer with zero delay evaluation board is designed for convenient setup and quick evaluation of the device. The evaluation board is designed to provide three outputs; two LVPECL outputs and one LVDS output. The loop-filter has been configured to data sheet recommendations; see the SY89538L data sheet for more details. For increased flexibility, the evaluation board has both an on board 16.6MHz series resonant crystal, and has provisions to accept an external reference and a zero delay feedback input. Both inputs feature on-board 50Ω input terminations. Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

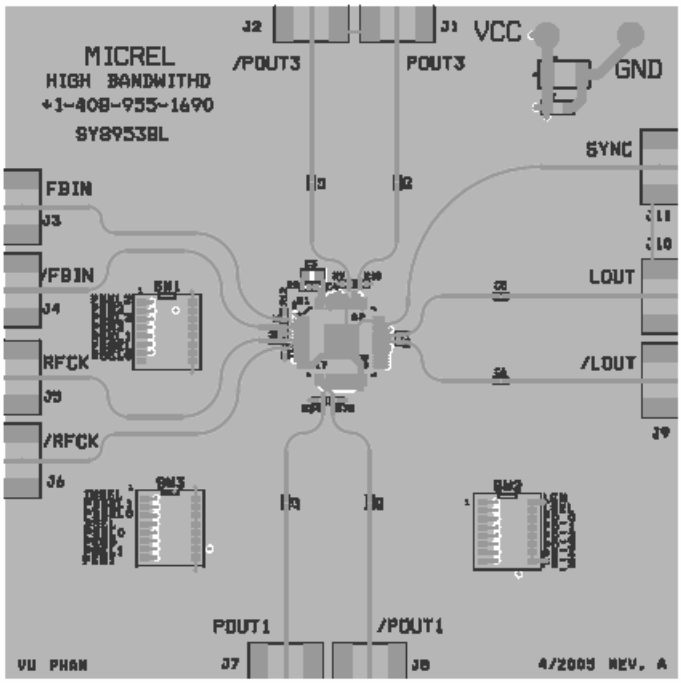
Features

- Evaluation board for the 3.3V, precision LVPECL and LVDS programmable multiple output bank clock synthesizer and fanout buffer with zero delay
- Requires a single 3.3V ±10% power supply
- On-board 50Ω input termination
- AC-coupled output configuration for direct interface to 50Ω equipment
- On board dip switches for ease of use

Related Documentation

- SY89538L 3.3V, Precision LVPECL and LVDS Programmable Multiple Output Bank Clock Synthesizer and Fanout Buffer with Zero Delay Data Sheet

Evaluation Board



Evaluation Board Description

Crystal and DC-Coupled Inputs

The evaluation board reference input (RFCK) is designed to accept a 9.325MHz to 756MHz DC-coupled reference input, and features an on-board 16.6MHz series resonant crystal. The evaluation board can also be configured in zero-delay mode (in which the output frequency is the same as the reference frequency) by feeding either the LVDS or LVPECL output into the zero-delay feedback input (FBIN). Both the DC-coupled reference and zero delay feedback inputs accepts any input logic standard including single-ended and differential TTL/CMOS, LVPECL, LVDS, HSTL, or SSTL signals. See the SY89538L data sheet for more details.

AC-Coupled Output

The LVPECL and LVDS outputs are AC-coupled designed to drive 50Ω systems

Evaluation Board Layout

PC Board Layout

The evaluation boards are constructed with FR4 material, coplanar in design, fabricated to minimize noise, and achieve high bandwidth, and minimize crosstalk.

Layer	Plane
L1	GND and 50 transmission line traces
L2	GND Plane
L3	Power Plane
L4	GND and DC signal traces

Table 1. Layer Stack

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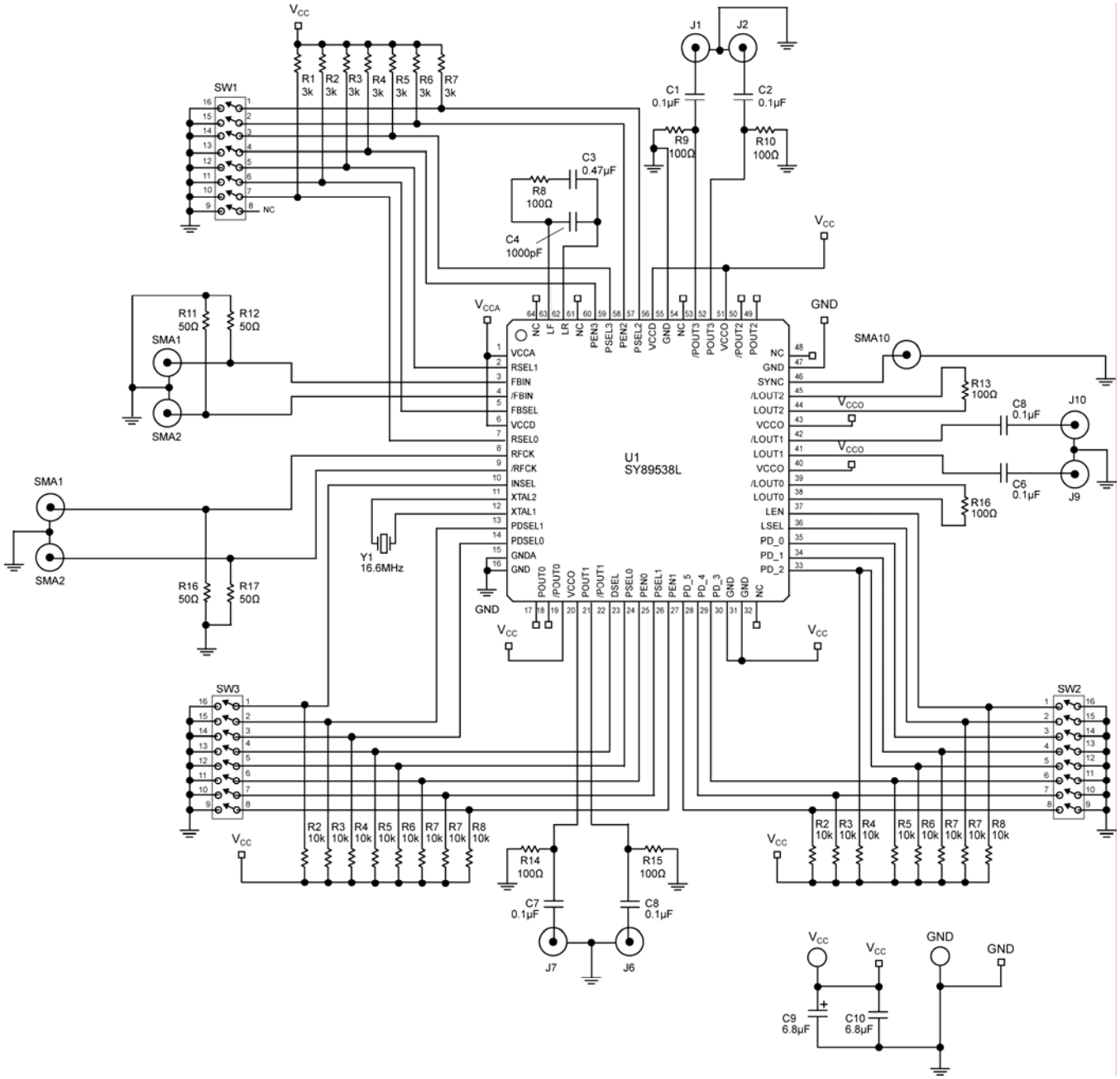
Evaluation Board



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Evaluation Board Setup

When the evaluation board is configured with FBSEL logic HIGH, the evaluation board acts a frequency multiplier and generates clock frequencies from 29.4MHz to 756MHz. When FBSEL is logic LOW, the evaluation board is configured in zero-delay mode. The evaluation board can be configured in three modes:

1. Mode 1: Reference Frequency Multiplier
2. Mode 2: Crystal Multiplier
3. Mode 3: Zero Delay

Power Supply Setup

1. Set TP1 (VCC) to 3.3V
2. Set TP2 (GND) to 0V

Mode 1: Reference Frequency Multiplier

1. Apply a 9.325MHz to 756MHz LVPECL signal to (RFCK) at SMA inputs (J5, J6) and program the Reference-Divider (RSEL1, RSEL0) with dip-switch SW1 [5,7] such that $f_{REF\text{-}DIV}$: 9.33MHz ≤ $f_{REF\text{-}DIV}$ ≤ 94.5MHz.
2. Set the Programmable-Divider PD [5:0] such that f_{VCO}: (2.35GHz ≤ f_{VCO} ≤ 3.02GHz) using dip-switch SW2 [3:8].

$$f_{VCO} = \left(\frac{\text{RFCK}}{\text{Ref}-\text{Divider}}\right) \times \text{Programmable}-\text{Divider} \times (\text{Pre}-\text{Divider}/2) \times (\text{Pre}-\text{Divider}/2)$$

3. Set dip-switch SW3 [1] to 0: (INSEL logic LOW).
4. Set dip-switch SW1 [6] to 1: (FBSEL logic HIGH).
5. Configure the output Pre-Divider using dipswitch SW3 [2, 3] = (PDSEL1, PDSEL0).
6. Configure the LVDS LOUT Post-Divider using dipswitch (SW2 [2, 1], SW3 [4]) = (LSEL, LEN, DSEL).
7. Configure the LVPECL POUT1 Post-Divider using dipswitch SW3 [7, 8, 4] = (PSEL1, PEN1, DSEL).
8. Configure the LVPECL LVPECL3 Post-Divider using dipswitch (SW1 [3, 4], SW3 [4]) = (PSEL3, PEN3, DSEL).

Mode 2: Crystal Multiplier

The on-board 16.6MHz crystal is a fundamental mode, series-resonant crystal.

1. Set dipswitch SW3 [1] to 1: (INSEL logic HIGH).
2. Set the Programmable-Divider PD [5:0] such that f_{VCO}: (2.35GHz ≤ f_{VCO} ≤ 3.02GHz) using dipswitch SW2 [3:8].

$$f_{VCO} = 16.6\text{MHz} \times \text{Programmable}-\text{Divider} \times (\text{Pre}-\text{Divider}/2) \times (\text{Pre}-\text{Divider}/2)$$

3. Set dip-switch SW1[6] to 1: (FBSEL logic HIGH)
4. Configure the output Pre-Divider using dipswitch SW3 [2, 3] = (PDSEL1, PDSEL0).
5. Configure the LVDS LOUT Post-Divider using dipswitch (SW2 [2, 1], SW3 [4]) = (LSEL, LEN, DSEL).
6. Configure the LVPECL POUT1 Post-Divider using dipswitch SW3 [7, 8, 4] = (PSEL1, PEN1, DSEL).
7. Configure the LVPECL LVPECL3 Post-Divider using dip-switch (SW1 [3, 4], SW3 [4]) = (PSEL3, PEN3, DSEL).

Mode 3: Zero-Delay Mode

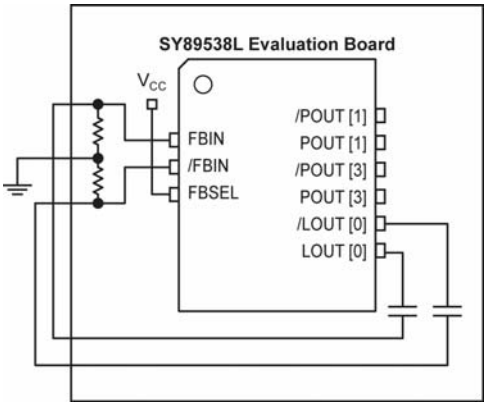

Figure 1a. Zero-Delay (LVDS Output)

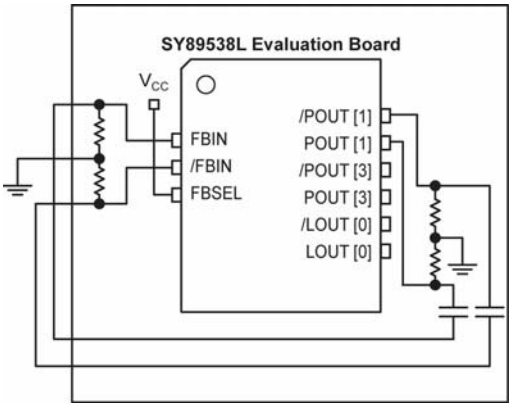

Figure 1b. Zero-Delay (LVPECL Output)

1. Apply a 9.325MHz to 756MHz LVPECL signal to (RFCK) at SMA inputs (J5, J6) and program the Reference-Divider (RSEL1, RSEL0) with dip-switch SW1 [5,7] such that $f_{REF-DIV}$: (9.33MHz ≤ $f_{REF-DIV}$ ≤ 94.5MHz.
2. Connect the output to the feedback input (FBIN), see Figure 1a and 1b.
3. Set dipswitch SW1 [6] to 0: (FBSEL logic LOW).
4. Configure the output Pre-Divider using dipswitch SW3 [2, 3] = (PDSEL1, PDSEL0).
5. Configure the LVDS LOUT Post-Divider using dipswitch (SW2 [2, 1], SW3 [4]) = (LSEL, LEN, DSEL).
6. Configure the LVPECL POUT1 Post-Divider using dipswitch SW3 [7, 8, 4] = (PSEL1, PEN1, DSEL).

Example:

The following example generates an output frequency of 120MHz from a 15MHz reference.

Parameter	Value	Units
f_{OUT}	120	MHz
f_{RFCK}	15	MHz
Ref-Divider	1	Integer
Feedback Programmable Divider	40	Integer
Pre-Divider	5	Integer
Post-Divider	2	Integer

Table 2. Divider Programming

$$f_{OUT} = \frac{f_{RFCK} \times \text{Feedback Programmable Divider} \times (\text{Div-by-2}) \times (\text{Div-by-2})}{\text{Ref. Divider} \times (\text{Div-by-2}) \times \text{PreDivider} \times \text{PostDivider})}$$

$$f_{OUT} = \frac{15\text{MHz} \times 40 \times 2 \times 2}{1 \times 2 \times 5 \times 2}$$

$$f_{OUT} = 120\text{MHz}$$

Dipswitch Programming

Pin8	Pin7	Pin6	Pin5	Pin4	Pin3	Pin2	Pin1
NC	RSEL0	FBSEL	RSEL1	PEN3	PSEL3	PEN2	PSEL2
X	1	1	1	1	0	1	0

Table 3. SW1 Dipswitch

Pin8	Pin7	Pin6	Pin5	Pin4	Pin3	Pin2	Pin1
PD5	PD4	PD3	PD2	PD1	PD0	LSEL	LEN
1	0	1	0	0	0	0	1

Table 4. SW2 Dipswitch

Pin8	Pin7	Pin6	Pin5	Pin4	Pin3	Pin2	Pin1
PEN1	PSEL1	PEN0	PSEL0	DSEL	PDSEL0	PDSEL1	INSEL
1	0	1	0	1	0	0	0

Table 5. SW3 Dipswitch

Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1, C2, C5, C6, C7, C8, C10	VJ0402G104KXQC	Vishay[1]	0.1μF, 10V, 10% Ceramic Capacitor, Size 0402, X5R Dielectric	7
C3	VJ0402Y474KXXC	Vishay[1]	0.47μF, 25V, 10% Ceramic Capacitor, Size 0402, X7R Dielectric	1
C4	VJ0402Y102KXXC	Vishay[1]	1000pF, 25V, 10% Ceramic Capacitor, Size 0402, X7R Dielectric	1
C9	293D685X0010	Vishay[1]	6.8μF, 25V, 10% Ceramic Capacitor, Size B, X7R Dielectric	6
R8	CRCW04021300F	Vishay[1]	130Ω, 1/16W, 5% Thick-film Resistor, Size 0603	1
R9, R10, R13, R14, R15, R34, R35	CRCW04021000F	Vishay[1]	100Ω, 1/16W, 5% Thick-film Resistor, Size 0402	7
R11, R12, R16, R17	CRCW040249R9F	Vishay[1]	50Ω, 1/16W, 5% Thick-film Resistor, Size 0402	4
SMA1-SMA11	142-0701-851	Johnson Components[2]	Jack Assembly End Launch SMA	11
SW1-SW3	CT2188LPST-ND	Digi-Key[3]	8-Position Dip Switch	3
TP1 (VCC)	5005K-ND	Keystone[4]	Test Point	1
TP2 (GND)	5005K-ND	Keystone[4]	Test Point	1
U1	**SY89538L**	**Micrel**[5]	**3.3V, Precision LVPECL and LVDS Programmable Multiple Output Bank Synthesizer and Fanout Buffer with Zero Delay**	1
Y1	AS-16.666-S-SMD-T-MI	Raltron[6]	Surface Mount 16.6MHz Crystal	1

Notes:

1. Vishay: www.vishay.com
2. Johnson Components: www.johnsoncomponents.com
3. DigiKey: www.digikey.com.
4. Keystone Electronics: www.keyelco.com.
5. **Micrel, Inc.**: **www.micrel.com.**
6. Raltron: www.raltron.com.

HBW Support

Hotline: 408-955-1690

Email Support: HBWHelp@micrel.com

Application Hints and Notes

For application notes on high-speed termination on PECL and LVPECL products, clock synthesizer products, SONET jitter measurement, and other High Bandwidth products go to Micrel Inc., website at http://www.micrel.com/. Once in Micrel's website, follow the steps below:

1. Click on "Product Info."
2. In the Applications Information Box, choose "Application Hints and Application Notes."

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